Listing of the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

1-33. (Cancelled)

34. (Previously Presented) A board-on-chip (BOC) and lead-on-chip (LOC) semiconductor device package assembly, comprising:

a semiconductor die;

a substrate to which the semiconductor die is attached;

adhesive die attach material disposed between the semiconductor die and the substrate, the adhesive die attach material directly abutting the substrate and the semiconductor die and attaching the semiconductor die and the substrate by a curing process comprising simultaneously applying uniform ambient pressure and heat to the semiconductor device package assembly to thereby form a reduced void die attach bondline at the interface between the adhesive die attach material and the semiconductor die having fewer voids than a die attach bond line not formed by simultaneous application of ambient pressure and heat.

35. (Original) The semiconductor device package assembly of claim 34 wherein the adhesive die attach material comprises a tri-layer die attach tape.

36. (Original) The semiconductor device package assembly of claim 34, further comprising a lead frame disposed between the semiconductor die and the substrate.

37. (Original) The semiconductor device package assembly of claim 34 wherein the semiconductor die is electrically coupled to conductive traces formed on the surface of the substrate through conductive bond wires.

38. (Original) The semiconductor device package assembly of claim 34 wherein the uniform pressure and heat are applied to the package assembly simultaneously for a length of time between 30 minutes and 4 hours.

39. (Original) The semiconductor device package assembly of claim 34 wherein the uniform pressure and heat are applied to the package assembly simultaneously, and the pressure applied is between about 30 and 250 pounds per square inch.

40. (Original) The semiconductor device package assembly of claim 34 wherein the uniform pressure and heat are applied to the package assembly simultaneously, and the applied heat has a temperature between about 100 °C and 200 °C.

41. (Original) The semiconductor device package assembly of claim 34 wherein the uniform pressure and heat are applied to the package assembly simultaneously for about 70 minutes, the pressure applied is about 125 pounds per square inch, and the heat applied has a temperature of about 165 °C.

42. (Previously Presented) A board-on-chip (BOC) and lead-on-chip (LOC) semiconductor device package assembly, comprising:

a semiconductor die;

a substrate having a first surface and a second surface, and an aperture disposed therethrough;

a pressure and heat cured adhesive die attach material disposed between the semiconductor die and the first surface of the substrate to adhere the die to the first surface of the substrate, the adhesive die attach material being cured by simultaneously applying ambient pressure and heat, and

a plurality of bond pads disposed on the semiconductor die and aligned with the aperture, the bond pads being electrically coupled to a corresponding plurality of conductive leads formed on the second surface of the substrate by bond wires passing through the aperture.

43. (Previously Presented) The semiconductor device package assembly of claim 42 wherein the adhesive die attach material comprises a tri-layer die attach tape.

44. (Previously Presented) The semiconductor device package assembly of claim 42, further comprising a lead frame disposed between the semiconductor die and the substrate.

45. (Previously Presented) The semiconductor device package assembly of claim 42 wherein the semiconductor die is electrically coupled to conductive traces formed on the surface of the substrate through conductive bond wires.

46. (Previously Presented) The semiconductor device package assembly of claim 42 wherein the uniform pressure and heat are applied to the package assembly simultaneously for a length of time between 30 minutes and 4 hours.

47. (Previously Presented) The semiconductor device package assembly of claim 42 wherein the uniform pressure and heat are applied to the package assembly simultaneously, and the pressure applied is between about 30 and 250 pounds per square inch.

48. (Previously Presented) The semiconductor device package assembly of claim 42 wherein the uniform pressure and heat are applied to the package assembly simultaneously, and the applied heat has a temperature between about 100 °C and 200 °C.

49. (Previously Presented) The semiconductor device package assembly of claim 42 wherein the uniform pressure and heat are applied to the package assembly simultaneously for about 70 minutes, the pressure applied is about 125 pounds per square inch, and the heat applied has a temperature of about 165 °C.